

1        (10)   ABSTRACT

2        Wafer-level chip-scale packaging technology is used for improving performance or  
3        reducing size of integrated circuits by using metallization of pad-to-bump-out beams  
4        as part of the integrated circuit structure. Chip-scale packaging under bump metal is  
5        routed to increase the thickness of top metal of the integrated circuit, increasing  
6        current carrying capability and reducing resistance. An exemplary embodiment for a  
7        power MOSFET array integrated structure is described. Another exemplary  
8        embodiment illustrated the use of chip-scale processes for interconnecting discrete  
9        integrated circuits.